AMENDMENTS TO THE SPECIFICATION:

Page 2, amend the paragraph beginning at line 19 as follows:

One solution is to simulate the software and the hardware parts together using commercial co-simulators. One notable benefit of this approach is the quality of the software component is much improved as the co-verification has eliminated errors that would otherwise only be found during system integration.

Page 3, amend the paragraph beginning at line 18 as follows:

The latest verification techniques make use of high-level verification languages (HVL) supported by tools such as Veristy's Specman Elite or ~~Sysnopsis'~~Synopsis' Vera. These provide good links to hardware simulation environments. Their purpose built test vector generation and coverage analysis tools make verification much easier and more thorough.

Page 12, amend the paragraph beginning at line 1 as follows:

A ~~kernal~~kernel 32 within the Seamless system provides memory management such that the memory accessible to both the software components and the hardware components may be modelled in a unified manner with appropriate parameters associated with different portions and with the software simulator and hardware ~~similator~~simulator reacting to accesses to different memory locations in different ways depending upon what is being simulated and what is represented by that memory.

Page 12, amend the paragraph beginning at line 33 and continuing to page 13, line 2 as follows:

The mapping between ***e*** and the global variables has to be considered. The default transfer size is 32 bits so for types that fit into a single 32-bit word, such as int, bool and char, the default mapping is correct. The connection offers the ability to change the ~~endianess~~endianness if required.

Page 13, amend the paragraph beginning at line 4 as follows:

Multi-word types are transferred as a list of ~~bit~~bits and then unpacked into an ***e*** structure. In these cases the ***e*** definitions must be padded to the correct number of bits to match the alignment in the software simulation.

Page 14, amend the paragraph beginning at line 10 as follows:

Within the simulation software a polling loop serves to monitor the start flag using step ~~26~~46 to detect when it is set. When the start flag is set, step 48 reads the associated variables from within the shared memory 40 and then the software stimulus specified is simulated at step 50 using the instruction set simulator and associated driver software. When this is complete, step 52 resets the start flag and processing on the simulation side returns to step 46.